CHARGE-TRAPPING MEMORY DEVICE USING HETEROSTRUCTURE OF MoS_2 FET ON $CrPS_4$

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We introduce a non-volatile charge-trapping memory device, based on the 2D heterostructure FET consisting of a MoS_2 channel and $CrPS_4$. Clockwise hysteresis behaviors in transfer curves measured at room temperature show a strong dependence on the thickness of $CrPS_4$, which is attributed to charge trapping at trap sites in the $CrPS_4$ layers [1]. Our heterostructure memory device exhibits both large memory windows up to 99.7 V and a high on/off current ratio ($3x10^5$) with good endurance during 625 cycles. Also, the non-volatile memory property is obtained because of its excellent trapping ability of trap sites in the $CrPS_4$. Especially, the memory window size can be effectively tuned from 7.6 V to 99.7 V with a high on/off current ratio by changing the sweep range of back gate voltage from 10 to 60 V at drain voltage, V_D=0.1 V. Such high performances of the charge trapping memory device with a simple heterostructure provide a promising route towards next-generation memory devices utilizing 2D materials.

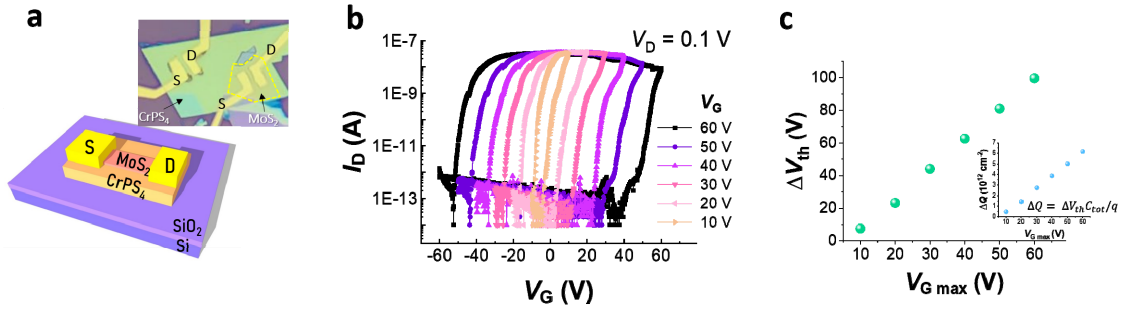

Fig. 1. **a.** Optical image and schematic of heterostructure device with MoS_2 channel on $CrPS_4$. **b.** Transfer curve of the device with different ranges of back gate voltage from 10 V to 60 V. **c.** Linear relationship between threshold voltage shift (ΔV_{th}) and gate voltage range ($V_{G\,max}$). The inset graph shows an amount of trapped charge in $CrPS_4$.

[1] S. Manzeli et al., Nat. Rev. Mater. **2**, 17033 (2017)